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<u>L25</u>	L23 and 11	0	<u>L25</u>
<u>L24</u>	L23 and 116	0	<u>L24</u>
<u>L23</u>	(719/329,332)![CCLS]	286	<u>L23</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L22</u>	116 and (plur\$8 or multiple or two or second or multi\$9 ) near5 thread\$3	85	<u>L22</u>
<u>L21</u>	L16 and 19	3	<u>L21</u>
<u>L20</u>	L16 and 18	8	<u>L20</u>
<u>L19</u>	L16 and 17	11	<u>L19</u>
<u>L18</u>	L16 and 16	157	<u>L18</u>
<u>L17</u>	L16 and 15	357	<u>L17</u>
<u>L16</u>	L15 and 11	511	<u>L16</u>
<u>L15</u>	(logic\$3 or bit near1 wise or "XOR" or exclusive) near5 (register\$1 or read\$5 or writ\$5)	96725	<u>L15</u>
<u>L14</u>	12 and 19	1	<u>L14</u>
<u>L13</u>	12 and 18	2	<u>L13</u>

<u>L12</u> 12 and 17	8	<u>L12</u>
<u>L11</u> 12 and 16	92	<u>L11</u>
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<u>L10</u> 12 and 15	282	<u>L10</u>
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<u>L8</u> (718/108 )! [CCLS]	274	<u>L8</u>
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<u>L5</u> (712/2-300)! [CCLS]	10394	<u>L5</u>
<u>L4</u> (712/2-300)! [CCLS]	35	<u>L4</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>		
<u>L3</u> L2 near25 (shar\$7 or common)	1	<u>L3</u>
<u>L2</u> L1 near25 (read\$6 or writ\$6)	339	<u>L2</u>
<u>L1</u> (remap\$7 or renam\$4) near8 register\$1 near15 (core\$1 or entit\$4 or thread\$4 or program\$6 or application\$1 or domain\$1 block\$1)	878	<u>L1</u>

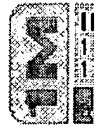
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Micro, IEEE, Volume: 20, Issue: 5, Sept.-Oct. 2000

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IEEE JNL

**2 Reducing register ports for higher speed and lower energy***Park, I.; Powell, M.D.; Vijaykumar, T.N.;*

Microarchitecture, 2002. (MICRO-35). Proceedings. 35th Annual IEEE/ACM International Symposium on, 18-22 Nov. 2002

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IEEE CNF

**3 Complexity-effective reorder buffer designs for superscalar processors***Kucuk, G.; Ponomarev, D.V.; Ergin, O.; Ghose, K.;*

Computers, IEEE Transactions on, Volume: 53, Issue: 6, June 2004

Pages:653 - 665

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IEEE JNL

**4 Register renaming for x86 superscalar design***Chang-Chung Liu; R-Ming Shiu; Chung-Ping Chung;*

Parallel and Distributed Systems, 1996. Proceedings., 1996 International Conference on, 3-6 June 1996

Pages:336 - 343

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IEEE CNF

**5 Testing the configurability of dynamic FPGAs***Park, N.; Ruiwale, S.J.; Lombardi, F.;*

Defect and Fault Tolerance in VLSI Systems, 2000. Proceedings. IEEE International Symposium on , 25-27 Oct. 2000

Pages:311 - 319

[\[Abstract\]](#) [\[PDF Full-Text \(464 KB\)\]](#) [IEEE CNF](#)**6 Assignment of storage values to sequential read-write memories***Gerez, S.H.; Woutersen, E.G.;*

Design Automation Conference, 1996, with EURO-VHDL '96 and Exhibition, Proceedings EURO-DAC '96, European , 16-20 Sept. 1996

Pages:302 - 308

[\[Abstract\]](#) [\[PDF Full-Text \(604 KB\)\]](#) [IEEE CNF](#)**7 Register write specialization register read specialization: a path to complexity-effective wide-issue superscalar processors***Seznec, A.; Toullec, E.; Rochecouste, O.;*

Microarchitecture, 2002. (MICRO-35). Proceedings. 35th Annual IEEE/ACM International Symposium on , 18-22 Nov. 2002

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[\[Abstract\]](#) [\[PDF Full-Text \(294 KB\)\]](#) [IEEE CNF](#)**8 A 14-port 3.8 ns 116-word 64b read-renaming register file***Asato, C.; Montoye, R.; Gmuender, J.; Wade Simmons, E.; Ike, A.; Zasio, J.;*

Solid-State Circuits Conference, 1995. Digest of Technical Papers. 42nd ISSCC 1995 IEEE International , 15-17 Feb. 1995

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*Seznec, A.; Toullec, E.; Rochecouste, O.;*

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